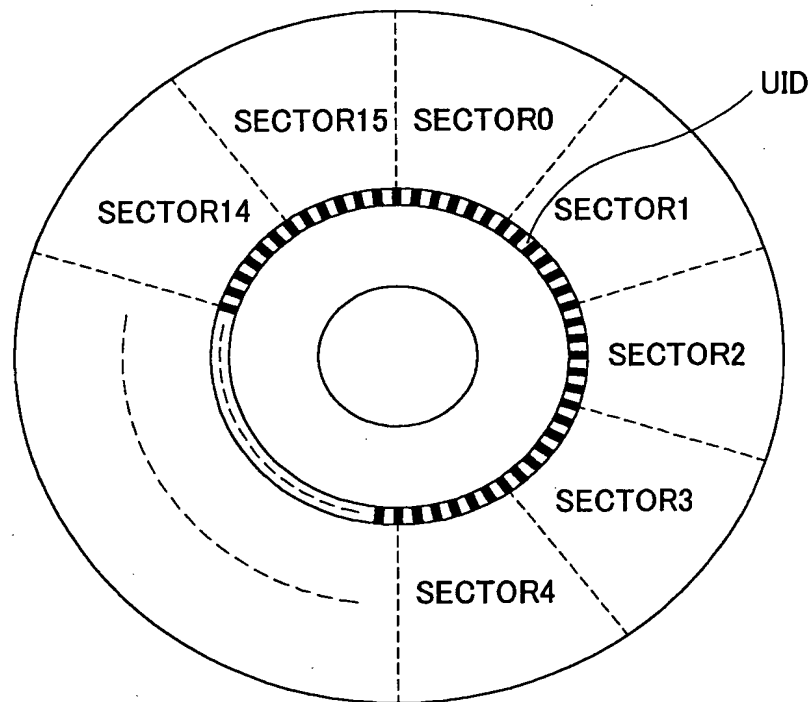


200



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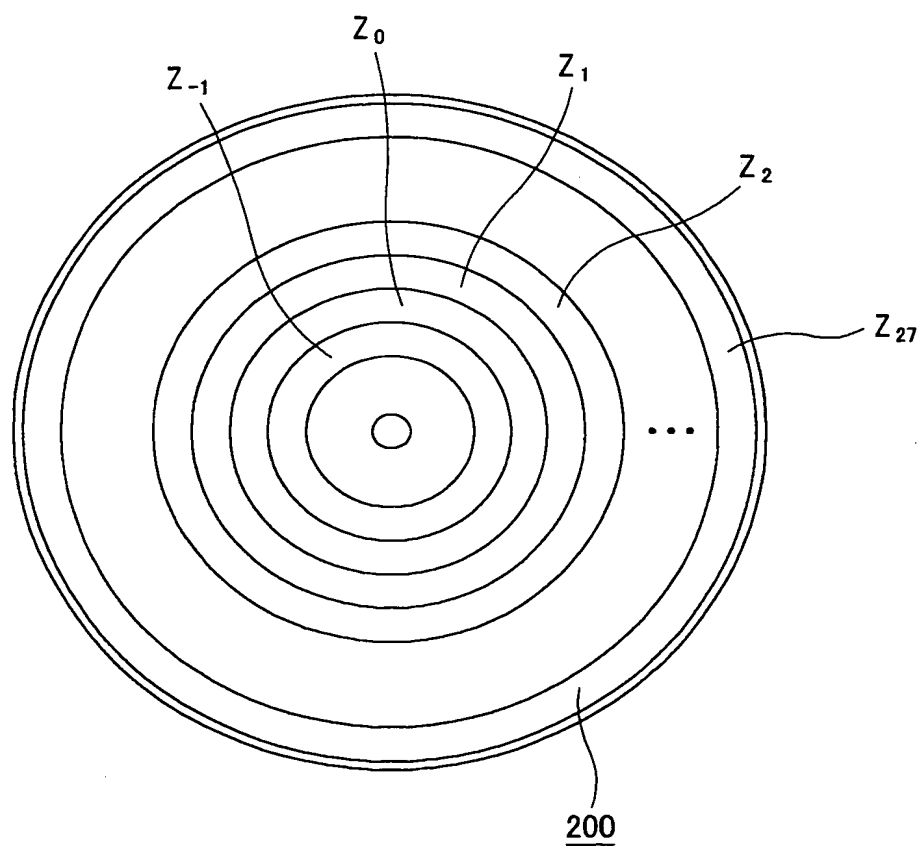


FIG. 2

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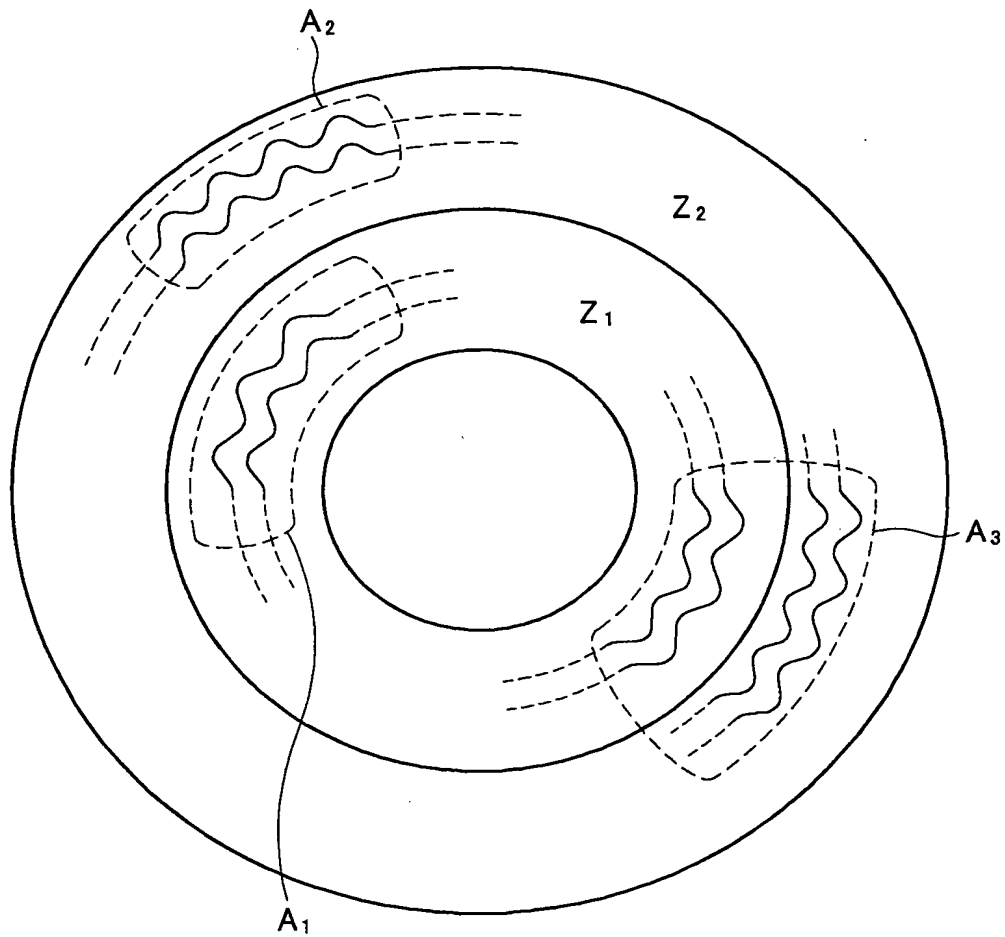


FIG. 3

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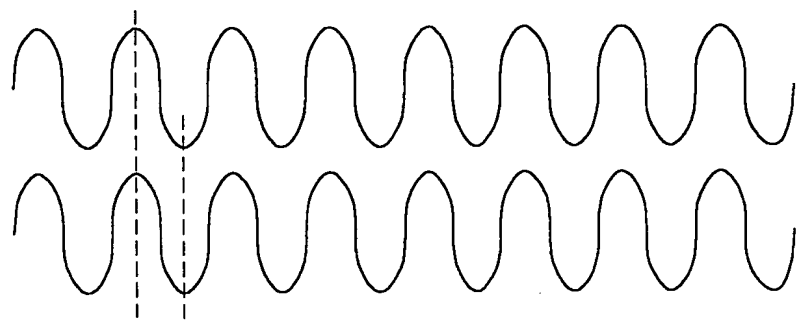


FIG. 4

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400

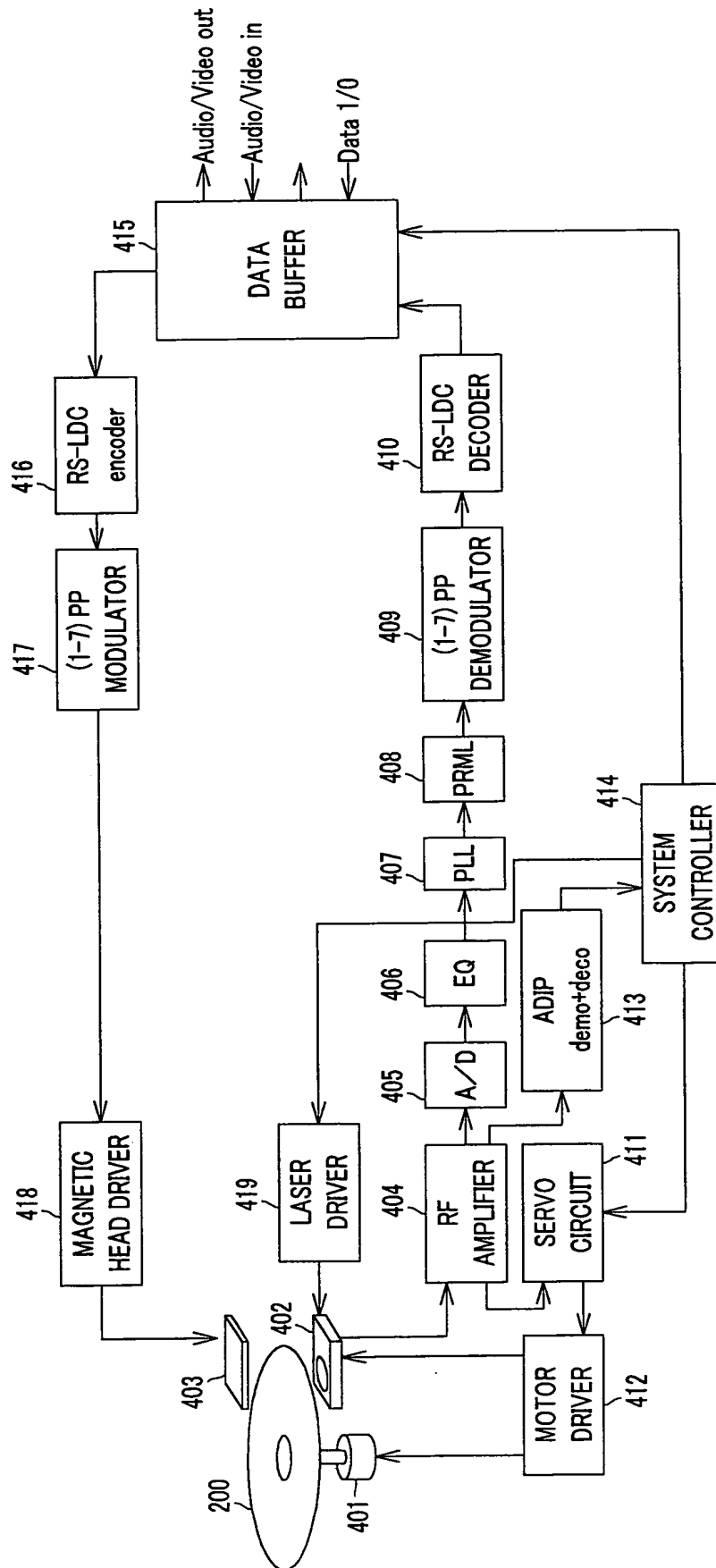


FIG.5

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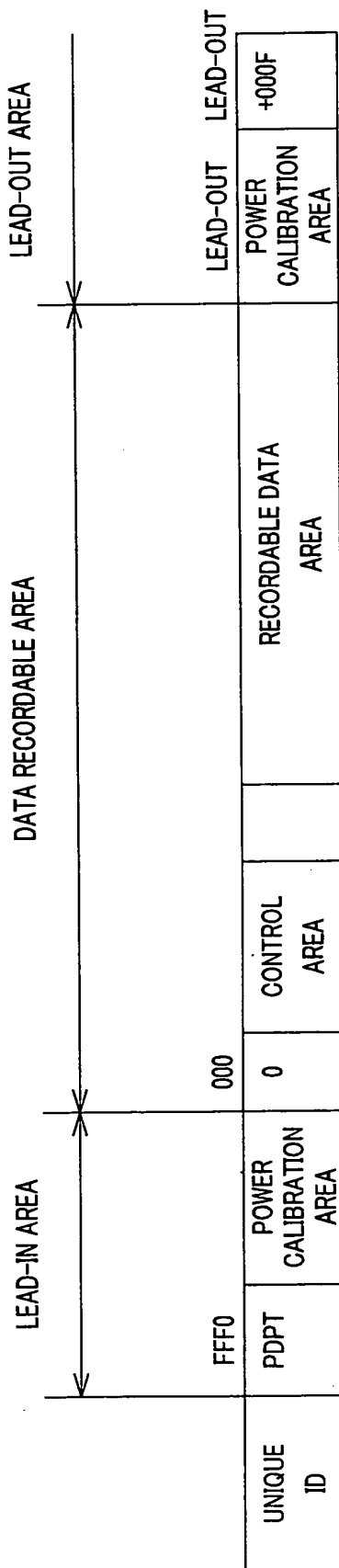


FIG.6

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sync 4bit	code H 8bit	code L 8bit	sector 4bit	BCH code parity 18bit
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FIG.7

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reproducing direction



header 1	header 2	header 3	header 4
CTD 1	CTD 2	CTD 3	unique ID1
unique ID2	unique ID3	unique ID4	unique ID5
unique ID6	unique ID7	unique ID8	unique ID9
unique ID10	unique ID11	unique ID12	unique ID13
unique ID14	unique ID15	unique ID16	EDC 1
ECC 1	ECC 2	ECC 3	ECC 4
ECC 5	ECC 6	ECC 7	ECC 8

FIG. 8

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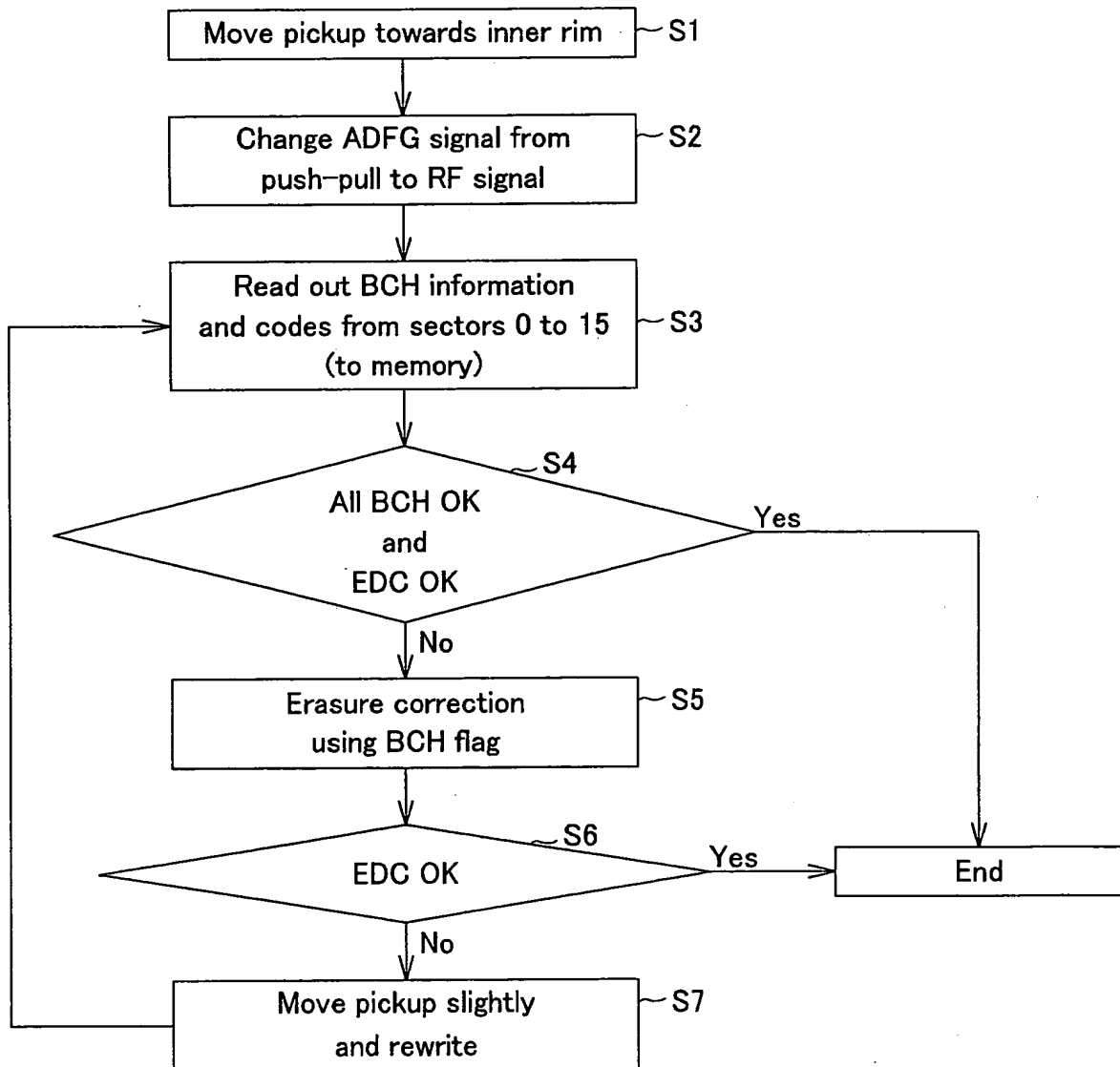


FIG.9

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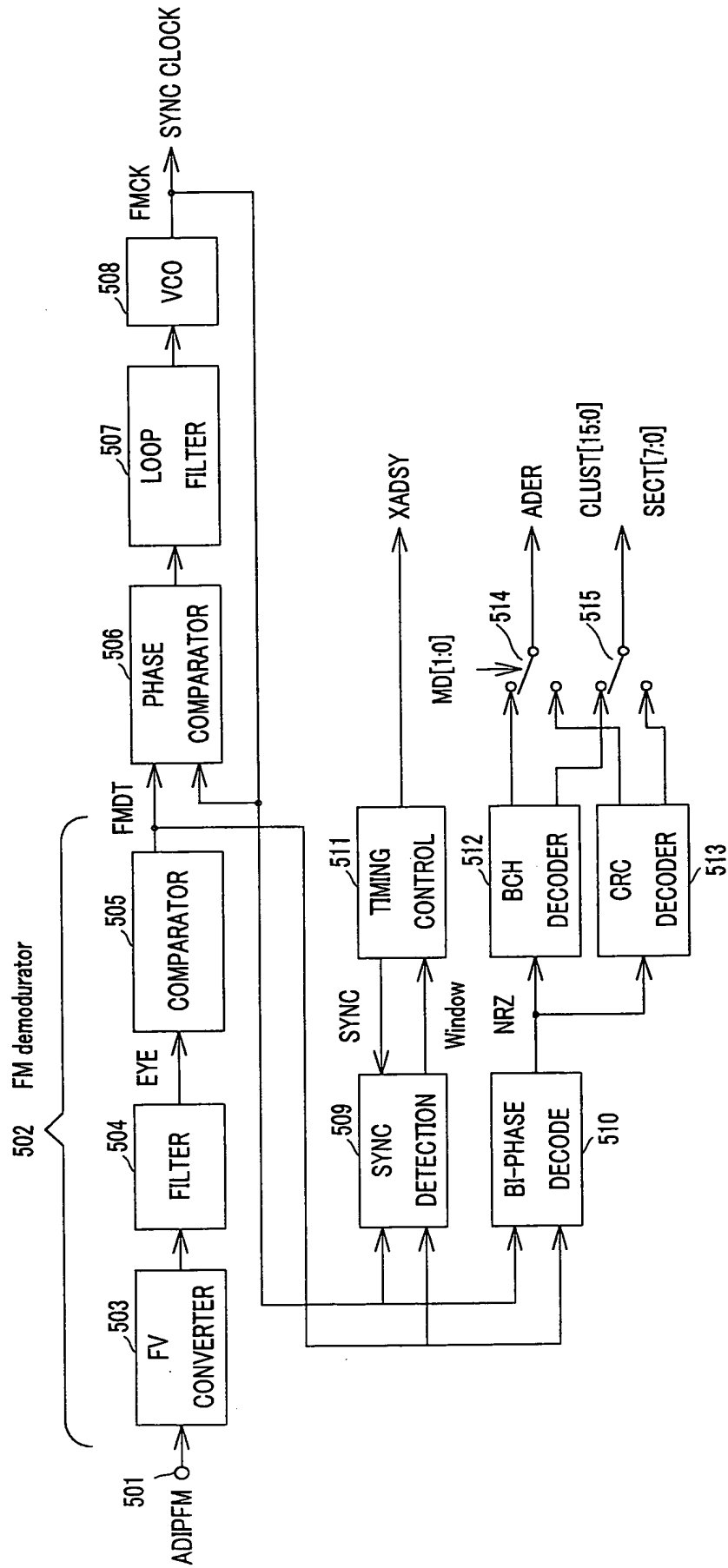


FIG.10

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FIG. 11A



FIG. 11B

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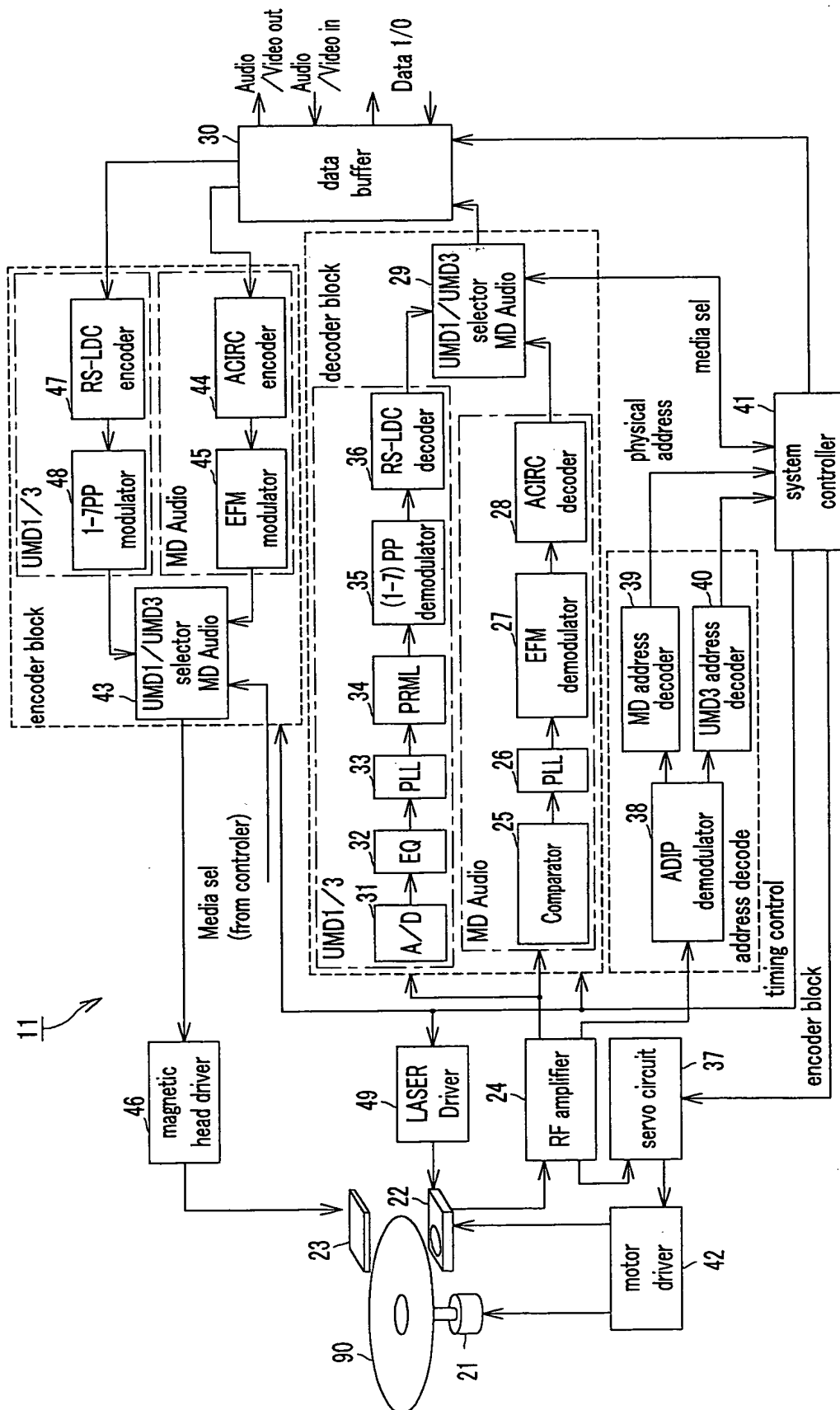


FIG.12

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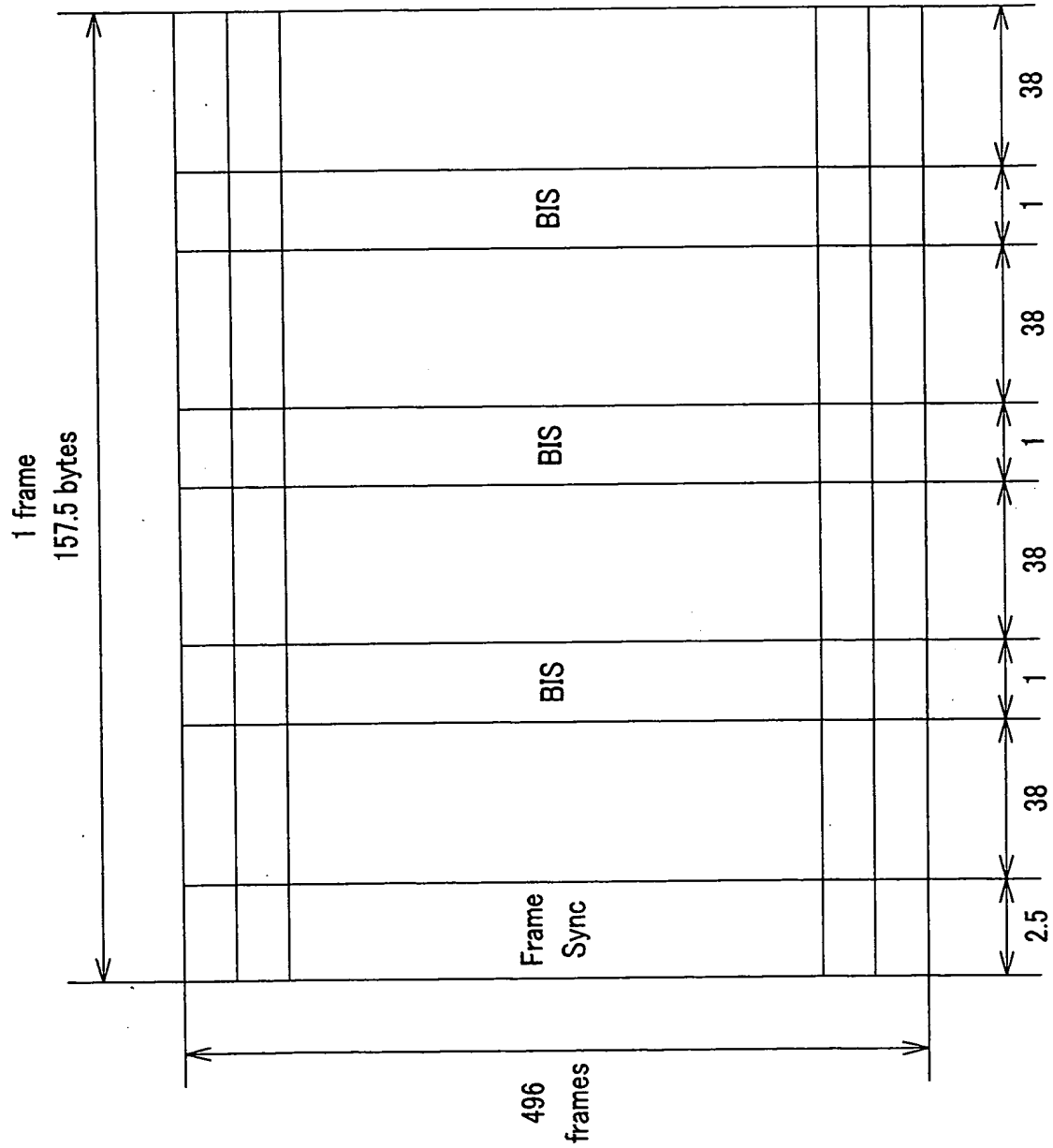


FIG.13

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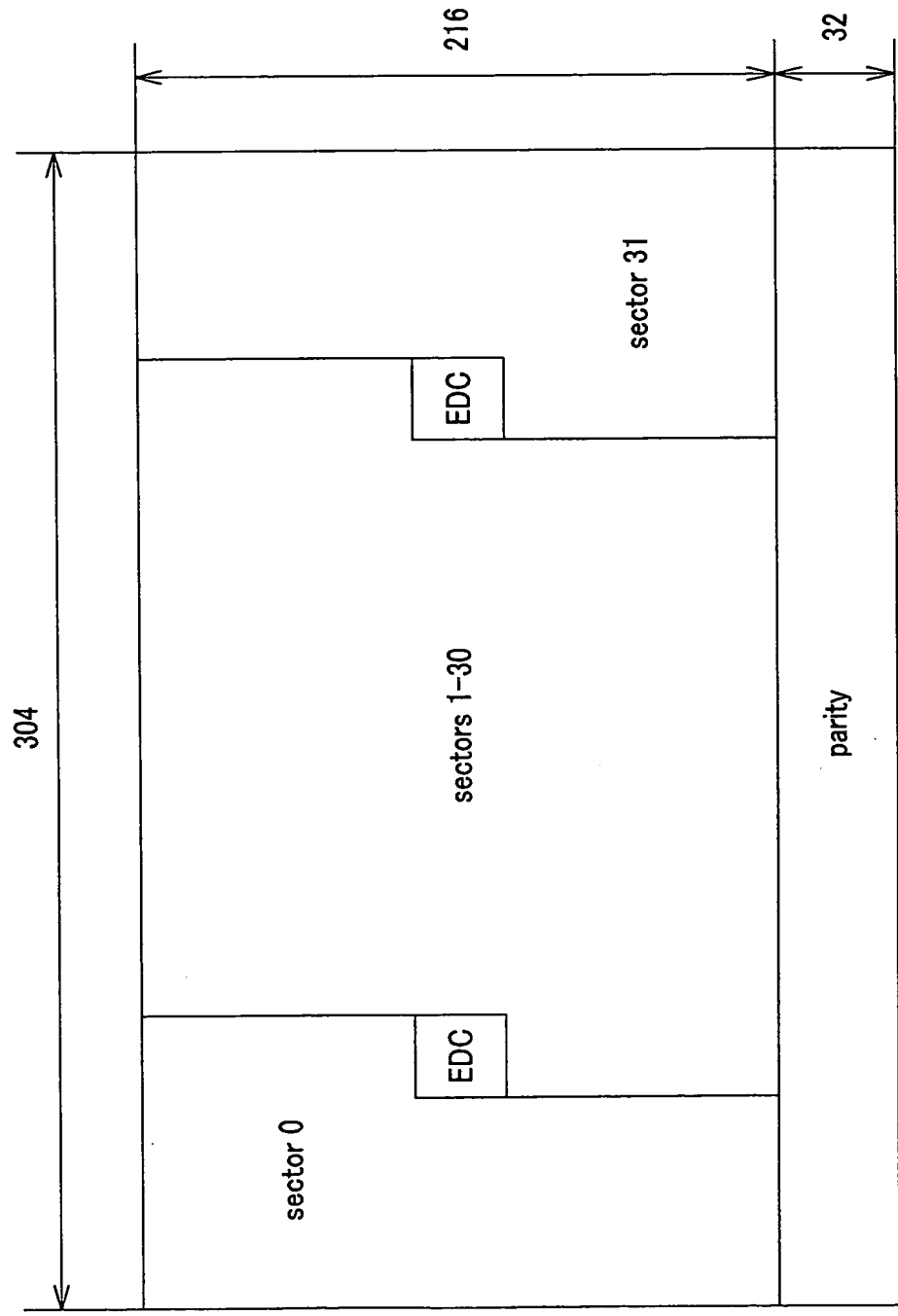


FIG.14

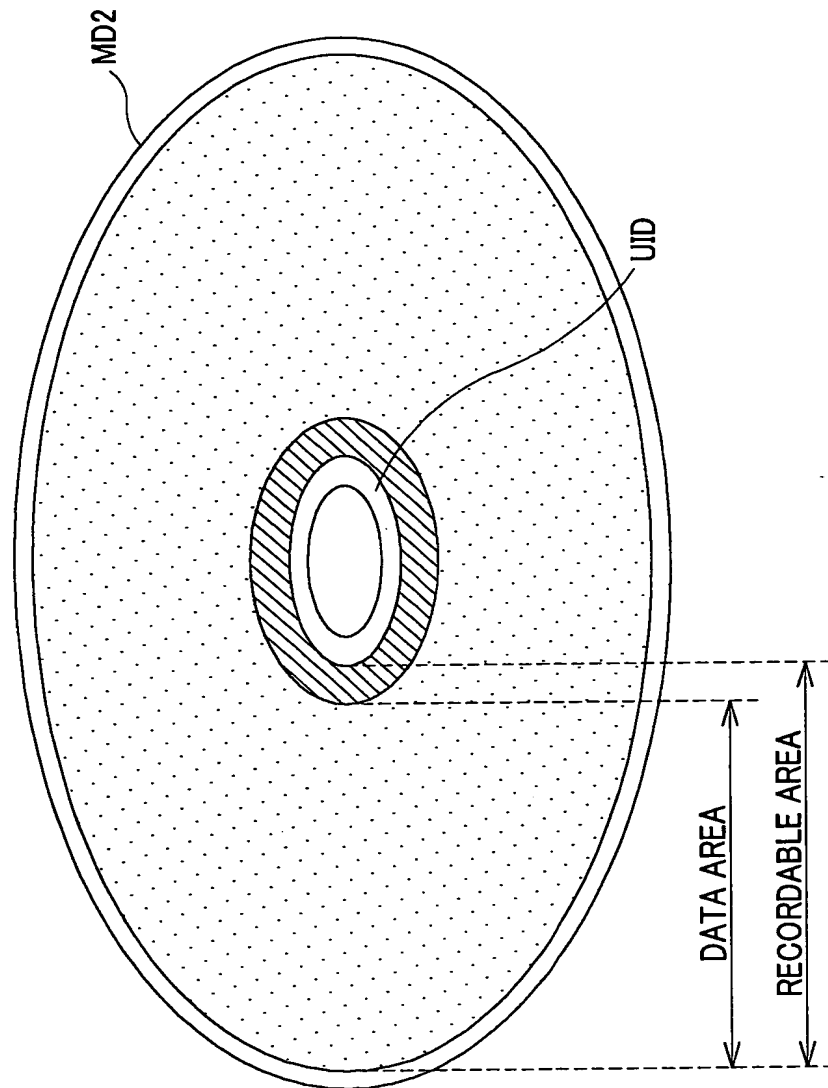


FIG. 15

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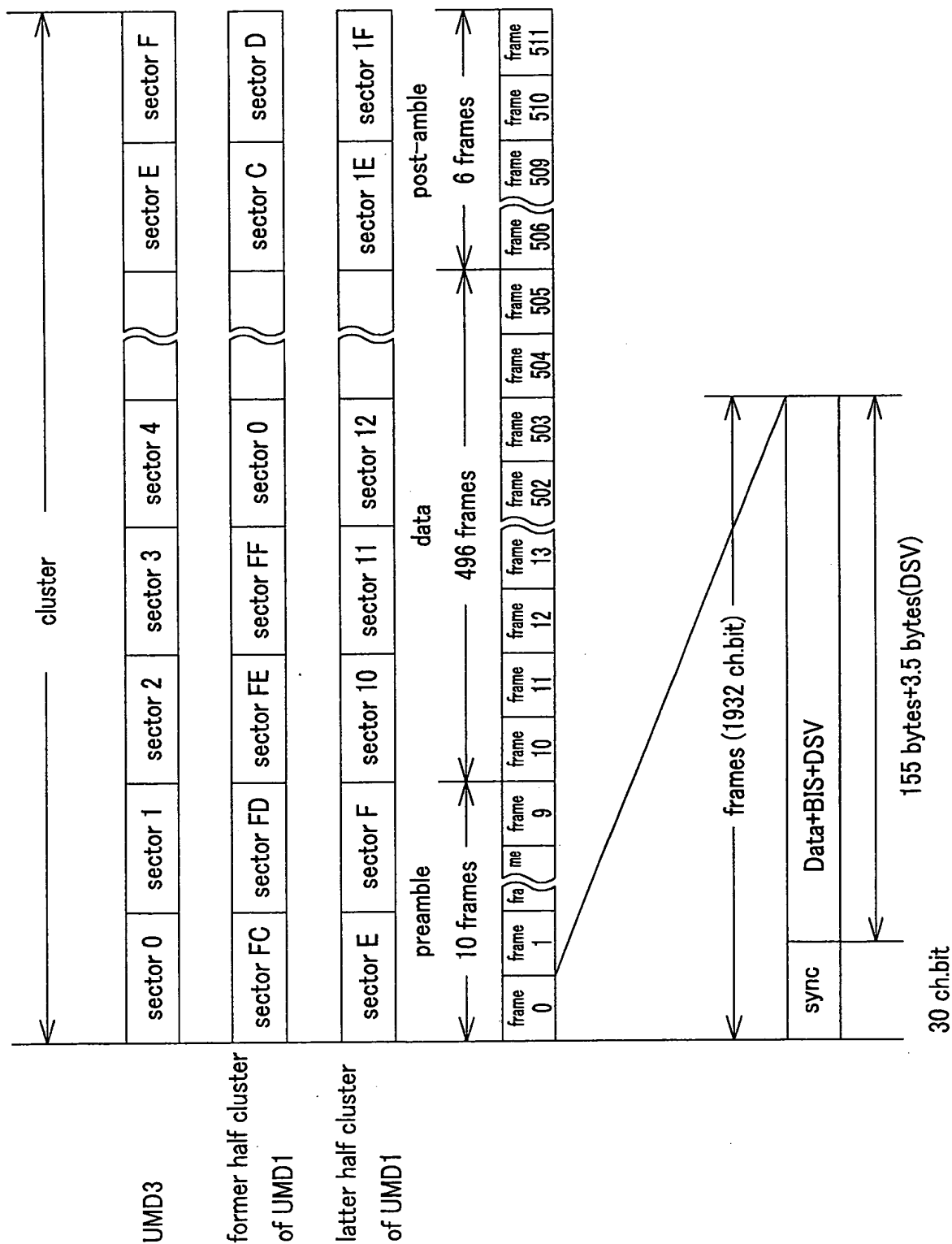


FIG.16

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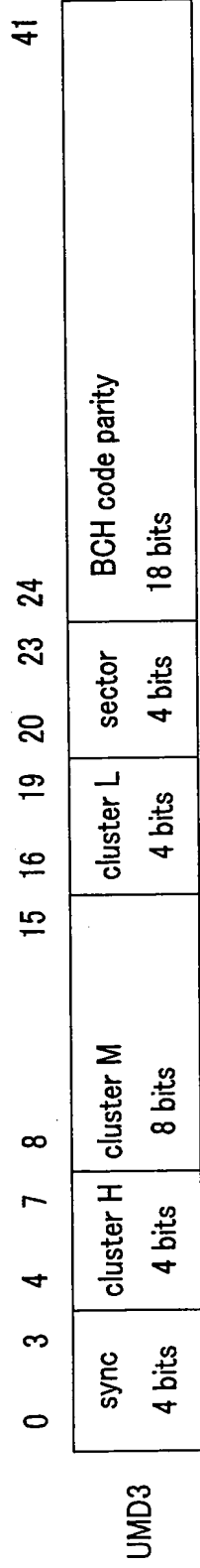


FIG.17A

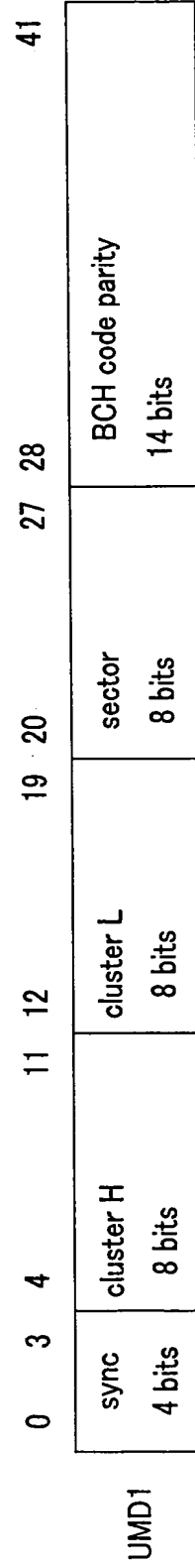


FIG.17B

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sync 4 bits	cluster H 8 bits	cluster L 8 bits	sector 4 bits	BCH code parity 18 bits
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FIG.18

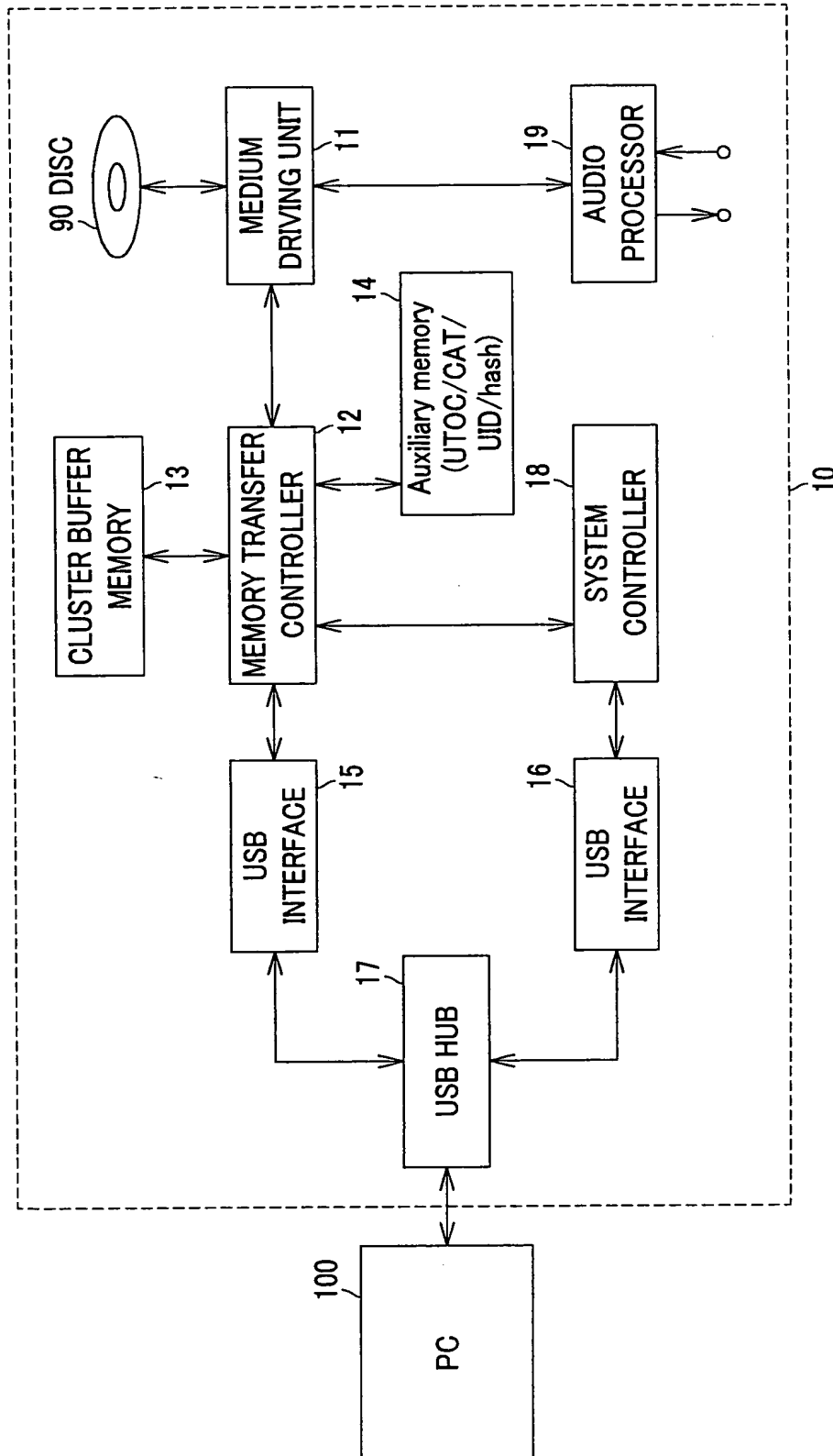


FIG.19

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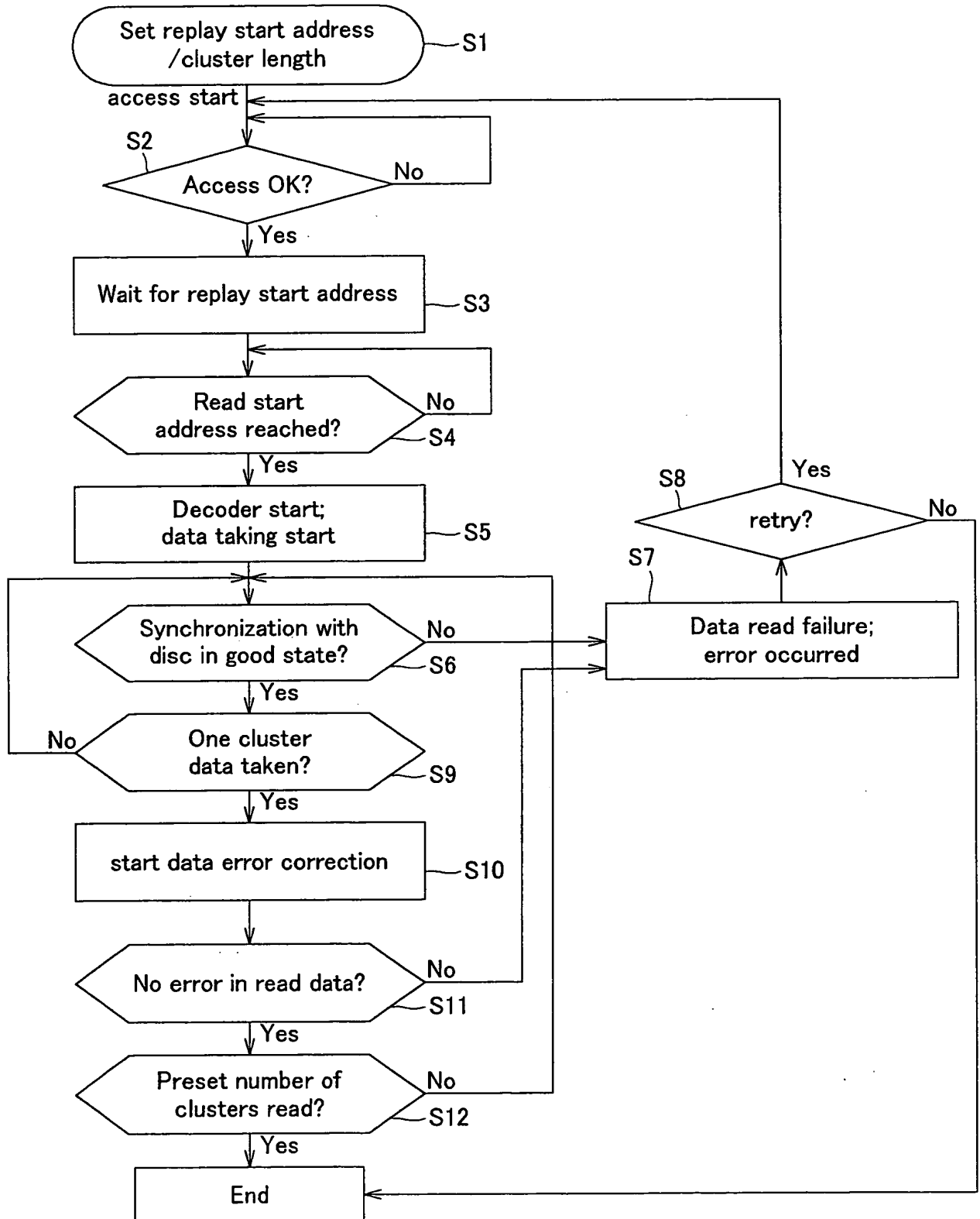


FIG 20

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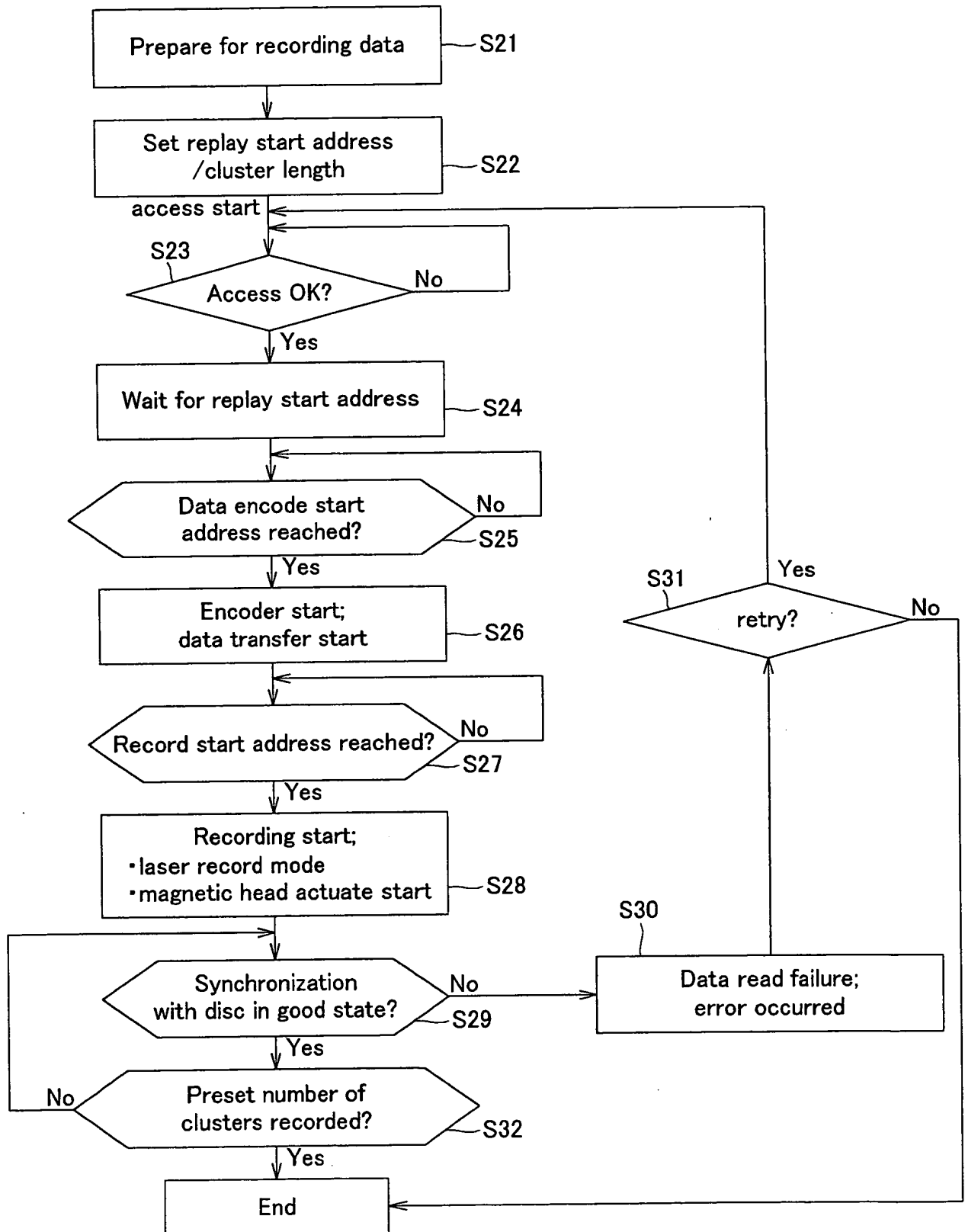


FIG.21

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